Multiple Choice Questions on 8086 Microprocessor

1. A microprocessor is a_____chip integrating all the functions of a CPU of a computer.
A. multiple B. single C. double D. triple
ANSWER: B
2. Microprocessor is a/an_____circuit that functions as the CPU of the compute
A. electronic B. mechanic C. integrating D. processing
ANSWER: A
3. Microprocessor is the_____of the computer and it perform all the computational tasks
A. main B. heart C. important D. simple
ANSWER: B
4. The purpose of the microprocessor is to control _____
A. memory B. switches C. processing D. tasks
ANSWER: A
5. The first digital electronic computer was built in the year_____
A. 1950 B. 1960 C. 1940 D. 1930
ANSWER: C
6. In 1960's texas institute invented _____
A. integrated circuits B. microprocessor C. vacuum tubes D. transistors
ANSWER: A
7. The intel 8086 microprocessor is a_____processor
A. 8 bit B. 16 bit C. 32 bit D. 4 bit
ANSWER: B
8. The microprocessor can read/write 16 bit data from or to _____
A. memory B. I /O device C. processor D. register
ANSWER: A
9. In 8086 microprocessor , the address bus is_____bit wide
A. 12 bit B. 10 bit C. 16 bit D. 20 bit
ANSWER: D
10. The work of EU is _____
A. encoding B. decoding C. processing D. calculations
ANSWER: B
11. The 16 bit flag of 8086 microprocessor is responsible to indicate _____
A. the condition of result of ALU operation B. the condition of memory
C. the result of addition D. the result of subtraction
ANSWER: A
12. The CF is known as _____
A. carry flag B. condition flag C. common flag D. single flag
.ANSWER: A
13. The SF is called as _____
A. service flag B. sign flag C. single flag D. condition flag
ANSWER: B
14. The OF is called as _____
A. overflow flag B. overdue flag C. one flag D. over flag
ANSWER: A

15. The IF is called as _____
A. initial flag B. indicate flag C. interrupt flag D. inter flag
ANSWER: C
16. The register AX is formed by grouping _____
A. AH & AL B. BH & BL C. CH & CL D. DH & DL
ANSWER: A
17. The SP is indicated by _____
A. single pointer B. stack pointer C. source pointer D. destination pointer
ANSWER: B
18. The BP is indicated by _____
A. base pointer B. binary pointer C. bit pointer D. digital pointer
ANSWER: A
19. The SS is called as _____
A. single stack B. stack segment C. sequence stack .D. random stack
ANSWER: B
20. The index register are used to hold _____
A. memory register B. offset address C. segment memory D. offset memory
ANSWER: A
21. The BIU contains FIFO register of size_____bytes
A. 8 B. 6 C. 4 D. 12
ANSWER: B
22. The BIU prefetches the instruction from memory and store them in _____
A. queue B. register C. memory D. stack
ANSWER: A
23. The 1 MB byte of memory can be divided into_____segment
A. 1 Kbyte B. 64 Kbyte C. 33 Kbyte D. 34 Kbyte
ANSWER: B
24. The DS is called as _____
A. data segment B. digital segment C. divide segment D. decode segment
ANSWER: A
25. The CS register stores instruction_____in code segment
A. stream B. path C. codes D. stream line
ANSWER: C
26. The IP is_____bits in length
A. 8 bits B. 4 bits C. 16 bits D. 32 bits
ANSWER: C
27. The push source copies a word from source to _____
A. stack B. memory C. register D. destination
ANSWER: A
28. LDs copies to consecutive words from memory to register and _____
A. ES B. DS C. SS D. CS
ANSWER: B
29. INC destination increments the content of destination by _____
A. 1 B. 2 C. 30 D. 41

ANSWER: A

30. IMUL source is a signed _____
A. multiplication B. addition C. subtraction D. division
ANSWER: A
31. _____destination inverts each bit of destination
A. NOT B. NOR C. AND D. OR
ANSWER: A
32. The JS is called as _____
A. jump the signed bit B. jump single bit
C. jump simple bit D. jump signal it
ANSWER: A
33. Instruction providing both segment base and offset address are called _____
A. below type .B. far type C. low type D. high type
ANSWER: B
34. The conditional branch instruction specify_____for branching
A. conditions B. instruction C. address D. memory
ANSWER: A
35. The microprocessor determines whether the specified condition exists or not by testing the _____
A. carry flag B. conditional flag C. common flag D. sign flag
ANSWER: B
36. The LES copies to words from memory to register and _____
A. DS B. CS C. ES D. DS
ANSWER: C
37. The_____translates a byte from one code to another code
A. XLAT B. XCHNG C. POP D. PUSH
ANSWER: A
38. The_____contains an offset instead of actual address
A. SP B. IP C. ES D. SS
ANSWER: B
39. The 8086 fetches instruction one after another from_____of memory
A. code segment B. IP C. ES D. SS
ANSWER: A
40. The BIU contains FIFO register of size 6 bytes called_____.
A. queue B. stack C. segment D. register
ANSWER: A
41. The_____is required to synchronize the internal operands in the processor CLK Signal
A. UR Signal B. Vcc C. AIE D. Ground
ANSWER: A
42. The pin of minimum mode AD0-AD15 has_____address
A. 16 bit B. 20 bit C. 32 bit D. 4 bit
ANSWER: B
43. The pin of minimum mode AD0- AD15 has _____data bus
A. 4 bit B. 20 bit C. 16 bit D. 32 bit
ANSWER: C
44. The address bits are sent out on lines through _____

A. A16-19 B. A0-17 C. D0-D17 D. C0-C17

ANSWER: A

45. _____is used to write into memory

A. RD B. WR C. RD / WR D. CLK

ANSWER: B

46. The functions of Pins from 24 to 31 depend on the mode in which_____is operating

A. 8085 B. 8086 C. 80835 D. 80845

ANSWER: B

47. The RD, WR, M/IO is the heart of control for a_____mode

A. minimum B. maximum C. compatibility mode D. control mode

ANSWER: A

48. In a minimum mode there is a_____on the system bus

A. single B. double C. multiple D. triple

ANSWER: A

49. If MN/MX is low the 8086 operates in_____mode

A. Minimum B. Maximum C. both (A) and (B) D. medium

ANSWER: B

50. In max mode, control bus signal So,S1 and S2 are sent out in_____form

A. decoded B. encoded C. shared D. unshared

ANSWER: B

51. The____bus controller device decodes the signals to produce the control bus signal

A. internal B. data C. external D. address

ANSWER: C

52. A_____Instruction at the end of interrupt service program takes the execution back to the interrupted program

A. forward B. return C. data D. line

ANSWER: B

53. The main concerns of the_____are to define a flexible set of commands

A. memory interface B. peripheral interface

C. both (A) and (B) D. control interface

.ANSWER: A

54. Primary function of memory interfacing is that the_____should be able to read from and write into register

A. multiprocessor B. microprocessor C. dual Processor D. coprocessor

ANSWER: B

55. To perform any operations, the Mp should identify the _____

A. register B. memory C. interface D. system

ANSWER: A

56. The Microprocessor places_____address on the address bus

A. 4 bit B. 8 bit C. 16 bit D. 32 bit

ANSWER: C

57. The Microprocessor places 16 bit address on the add lines from that address by _____ register should be selected

A. address B. one C. two D. three

ANSWER: B

58. The_____of the memory chip will identify and select the register for the EPROM
A. internal decoder B. external decoder C. address decoder D. data decoder
ANSWER: A
59. Microprocessor provides signal like_____to indicate the read operatio
A. LOW B. MCMW C. MCMR D. MCMWR
ANSWER: C
60. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the_____chip.
A. single B. memory C. multiple D. triple
ANSWER: B
61. The remaining address line of_____bus is decoded to generate chip select signal
A. data B. address C. control bus D. both (a) and (b)
ANSWER: B
62. _____signal is generated by combining RD and WR signals with IO/M
A. control B. memory C. register D. system
ANSWER: A
63. Memory is an integral part of a_____system
A. supercomputer B. microcomputer
C. mini computer D. mainframe computer
ANSWER: B
64. _____has certain signal requirements write into and read from its registers
A. memory B. register C. both (a) and (b) D. control
ANSWER: A
65. An_____is used to fetch one address
A. internal decoder B. external decoder C. encoder D. register
ANSWER: A
66. The primary function of the_____is to accept data from I/P devices
A. multiprocessor B. microprocessor C. peripherals D. interfaces
ANSWER: B
67. _____signal prevent the microprocessor from reading the same data more than one
A. pipelining B. handshaking C. controlling D. signaling
ANSWER: B
68. Bits in IRR interrupt are _____
A. reset B. set C. stop D. start
ANSWER: B
69. _____generate interrupt signal to microprocessor and receive acknowledge
A. priority resolver B. control logic
C. interrupt request register D. interrupt register
ANSWER: B
70. The_____pin is used to select direct command word
A. A0 B. D7-D6 C. A12 D. AD7-AD6
ANSWER: A
71. The_____is used to connect more microprocessor
A. peripheral device B. cascade C. I/O devices D. control unit
ANSWER: B

72. CS connect the output of _____
A. encoder B. decoder C. slave program D. buffer
ANSWER: B
73. In which year, 8086 was introduced?
A. 1978 B. 1979 C. 1977 D. 1981
ANSWER: A
74. Expansion for HMOS technology_____
A. high level mode oxygen semiconductor
B. high level metal oxygen semiconductor
C. high performance medium oxide semiconductor
D. high performance metal oxide semiconductor
ANSWER: D
75. 8086 and 8088 contains_____transistors
A. 29000 B. 24000 C. 34000 D. 54000
ANSWER: A
76. ALE stands for _____
A. address latch enable B. address level enable
C. address leak enable D. address leak extension
ANSWER: A
77. What is DEN?
A. direct enable B. data entered C. data enable D. data encoding
ANSWER: C
78. In 8086, Example for Non maskable interrupts are_____.
A. TRAP B. RST6.5 C. INTR D. RST6.6
ANSWER: A
79. In 8086 the overflow flag is set when_____.
A. the sum is more than 16 bits.
B. signed numbers go out of their range after an arithmetic operation.
C. carry and sign flags are set.
D. subtraction
ANSWER: B
80. In 8086 microprocessor the following has the highest priority among all type interrupts?
A. NMI B. DIV 0 C. TYPE 255 D. OVER FLOW
ANSWER: A
81. In 8086 microprocessor one of the following statements is not true?
A. coprocessor is interfaced in max mode. B. coprocessor is interfaced in min mode.
C. I /O can be interfaced in max / min mode. D. supports pipelining
ANSWER: B
82. Address line for TRAP is?
A. 0023H B. 0024H C. 0033H D. 0099H
ANSWER: B
83. Access time is faster for_____.
A. ROM B. SRAM C. DRAM D. ERAM
ANSWER: B

84. The First Microprocessor was_____.

A. Intel 4004 B. 8080 C. 8085 D. 4008

ANSWER: A

85. Status register is also called as_____.

A. accumulator B. stack C. counter D. flags

ANSWER: D

86. Which of the following is not a basic element within the microprocessor?

A. Microcontroller B. Arithmetic logic unit (ALU)

C. Register array D. Control unit

Ans.: A

87. Which method bypasses the CPU for certain types of data transfer?

A. Software interrupts B. Interrupt-driven I/O

C. Polled I/O D. Direct memory access (DMA)

Ans.: D

88. Which bus is bidirectional?

A. Address bus B. Control bus

C. Data bus D. None of the above

Ans.: C

89. The first microprocessor had a(n)_____.

A. 1 – bit data bus B. 2 – bit data bus

C. 4 – bit data bus D. 8 – bit data bus

Ans.: C

90. Which microprocessor has multiplexed data and address lines?

A. 8086 B. 80286 C. 80386 D. Pentium

Ans.: A

91. Which is not an operand?

A. Variable B. Register C. Memory location D. Assembler

Ans.: D

92. Which is not part of the execution unit (EU)?

A. Arithmetic logic unit (ALU) B. Clock

C. General registers D. Flags

Ans.: B

93. A 20-bit address bus can locate_____.

A. 1,048,576 locations B. 2,097,152 locations

C. 4,194,304 locations D. 8,388,608 locations

Ans.: A

94. Which of the following is not an arithmetic instruction?

A. INC (increment) B. CMP (compare)

C. DEC (decrement) D. ROL (rotate left)

Ans.: D

95. During a read operation the CPU fetches_____.

A. a program instruction B. another address

C. data itself D. all of the above

Ans.: D

96. Which of the following is not an 8086/8088 general-purpose register?

A. Code segment (CS) B. Data segment (DS)

C. Stack segment (SS) D. Address segment (AS)

Ans.: D

97. A 20-bit address bus allows access to a memory of capacity

A. 1 MB B. 2 MB C. 4 MB D. 8 MB

Ans.: A

98. Which microprocessor accepts the program written for 8086 without any changes?

A. 8085 B. 8086 C. 8087 D. 8088

Ans.: D

99. Which group of instructions do not affect the flags?

A. Arithmetic operations B. Logic operations

C. Data transfer operations D. Branch operations

Ans.: C

100. The result of MOV AL, 65 is to store

A. store 0100 0010 in AL B. store 42H in AL

C. store 40H in AL D. store 0100 0001 in AL

Ans.: D